REMARKS

Claims 1-18 are the in application. Claims 3-5, 10-12 and 18 were objected to but indicated as allowable over the cited art.

Applicant has amended the specification and certain of the claims in response to the informalities noted by the Examiner. Applicant submits that acronyms are now sufficiently defined in the specification, and that the informalities noted by the Examiner are addressed by the amendments made herein.

Applicant also has taken the opportunity to clarify the wording of the claims and to correct typographical errors and the like. These amendments are unrelated to the substantive rejections of the Examiner. No new matter has been added.

Applicant respectfully traverses the rejection of claims 1, 2, 6-9, and 13-17 in view of USP 4,961,135 (Uchihori). Applicant submits that, properly interpreted, Uchihori is readily distinguishable from Applicant's invention.

In accordance with the present invention, first and second TLBs (translation lookaside buffers) are provided in the processor (or in the design data module for the processor, etc.). As described in detail in Applicant's specification, first and second TLBs are utilized in Applicant's invention for more efficient and flexible address translation. As described in connection with Fig.1 of Applicant's currently amended disclosure, the first TLB and the second TLB are independent TLBs, and can be different physically and functionally. As illustrated in Figs. 2 and 3 of Applicant's disclosure, even the ENTRY numbers may differ in the first TLB and second TLB. Thus, first and second TLB's in Applicant's claims mean just that - they are two distinct TLBs. Since the first TLB and the second TLB are independent, for example, entry replacement of UTLB at the time of replacement of UTLB is performed within UTLB, and is not related to DTLB.

The Examiner, however, indicated that the first TLB and the second TLB of the present invention are anticipated by TLBs (75A and 75B) of Fig. 9 of the Uchihori reference. This, respectfully, is incorrect. TLBs (75A and 75B) of Uchihori are in reality a single TLB structure of the so-called 2 way set associative configuration. Although the TLB of the well-known set associative configuration is structured to have a plurality ways (in Uchihori, there are two,

designed side A and side B, etc.), this is fundamentally different from a plurality of TLBs as in Applicant's invention.

In accordance with Uchihori's set associative structure, in each way, the number of entries is the same, and when the entry of the TLB is replaced, selection of which way to replace an entry is made (that is, TLB 75A and 75B are part of the same TLB structure and are not independent or two separate TLBs). For example, in connection with Fig. 13A of Uchihori, an explanation is provided that the REPLACE object is chosen from one of the sides, TLB (A) or TLB (B). TLB(A) and TLB(B) are not first and second TLBs as in Applicant's invention. Fourway set associative structures also are known in the art, and four sets of structures similar to 75A and 75B are arranged in one TLB. In such structures, one of the four outputs is selected and outputted. Nonetheless, it would be understand by one of skill in the art that this structure is a four-way set associative structure and not four separate and distinct TLBs.

Accordingly, Applicant submits that the presently claimed invention is neither disclosed in nor suggested by Uchihori. Withdrawal of the rejection and allowance is respectfully requested.

If there are any questions, Applicant's attorney requests an opportunity to discuss such questions with the Examiner by way of a telephone or in-person interview.

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Reconsideration and allowance is requested.

Respectfully submitted,

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I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated above.